Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 01/01/06 – 03/31/06

Project: NIH/NINDS **Contract-No.** HHSN265200423621C
Date: 01/01/06-03/31/06
Contact details:

Prof. Dr.-Ing. Florian Solzbacher, Ph.D.
Dept. of Electrical Engineering and Computing
Director Microsystems Laboratory
University of Utah
Department of Electrical and Computer Engineering
MEB 3280
Tel.: (801) 581 7408 / 6941 (secretary)
Fax: (801) 581 5281
Email: solzbach@ece.utah.edu
URL: http://www.microsystems.utah.edu

Table of contents

I. Executive Summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

The objective of the sixth contract quarter (Q6) as proposed was to:

a) Optimize the backside (rerouting metallization) to improve adhesion and support more reliable flip-chip bonding.
b) Investigate new polishing procedures to support wafer level Utah Electrode Array fabrication.
c) Implant a fully functional device in a cat and acquire data for a month.
d) Bench-top testing of the second generation signal processing chip and initial acute in-vivo recordings from mammalian cortex (4 weeks of data)
e) Continue design, construction, and testing of external interface components (i.e. power supply coil, forward telemetry transmitter, software controls, etc).
f) Continue flip-chip integration work with addition of surface mount devices (SMDs) and custom made coil spacers to the integrated device.
g) Continue leakage current, impedance spectroscopy, adhesion and dissolution long term tests of SiC and Parylene encapsulation in buffer solution and subsequent further development of Parylene and SiC coating processes, materials characterization (material composition, electrical and chemical properties)

Throughout the sixth quarter, all of the above mentioned objectives were completely accomplished with the exception of item c): initial acute recording and stimulation experiments were made; chronic recordings are in progress.

II. Activity Summary

Key results for project period (Q 6) (work packages)

- Fabrication of UEA test and hot chips: fabrication of UEAs was continued. The Microsystems Lab is now in a production mode where new wafers are fed into the process every week. The fabrication process for the rerouting metallization was tested. The new metallization schemes are being tested. Work is in progress for optimizing fabrication processes and implementing wafer scale processes.
- Development and fabrication of electronics and communications module: The external interface circuits have been built and are being tested. The 2nd version signal processor is being tested. The investigation of thermal impact of the integrated array on the brain tissue has been started.
- Development and fabrication of PI/BCB coil: Design of the PI coils has been finalized and fully characterized.
- Flip-chip bonding and assembly: Individual integration concepts have been applied and tested.
- Hermetic encapsulation and layer coating: The adhesion between parylene and the device materials has been improved by optimizing the surface modification techniques
- Testing and validation of probe systems: Initial next generation UEAs with wireless power supply and/or data transmission were tested in benchtop and (acute) in-vivo rat cortex, chronic recording experiments in felines were prepared.

Meetings/presentations during project period (Q 6)

- Telephone conference with IZM

- Technical meeting with IZM personnel at the University of Utah
- Presentations and lab tours by IZM personnel at the University of Utah
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q 6)

- Further processing of previously submitted invention disclosures. Initiation of patent search on neuroprosthetic devices to identify the profile for further invention disclosures, e.g. for the signal processor and coil design.

Organizational accomplishments (Q 6)

- Initiation of collaboration with Brigham Young University for surface analysis of samples
- Established and implemented protocols for good manufacturing practices and good laboratory procedures (GMP/GLP) in preparation of potential later FDA approval.

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

During the past quarter there have been several further improvements in the probe fabrication processes. The bottle neck manufacturing processes were identified and were successfully duplicated for faster production of arrays. Processes further optimized on a wafer scale include dicing, polishing, and etching. The wire bonder is being customized to be used to bond wires on the wired-arrays.

Experimental Results

Dicing: in addition to the 'K&S' saw that was previously being used for dicing, we have created additional safety and redundancy in our process by transferring the process to a second (new) 'Disco' saw. The 'Disco' saw was characterized and parameters optimized to obtain identical results as the 'K&S' saw. Currently, backside dicing is being performed on both the saws. Fig. 1 and Fig. 2 show optical microscopy images of the wafers diced with the 'Disco' saw.

Tab. 1. Specifications of the blade and parameters used on the Disco DAD 641 saw for backside dicing

Blade Used	Nickel bound blade
Blade specifications	51.4 mm (O.D), 40.0 mm (I.D), 50 um thick
Diamond grit size	3-6 um
Dicing Machine	Disco DAD 641
Dicing Specifications	Spindle speed: 30,000 rpm Feed speed: 3000 mm/s Cut depth: 300-500 um Kerf width: 80-100 um

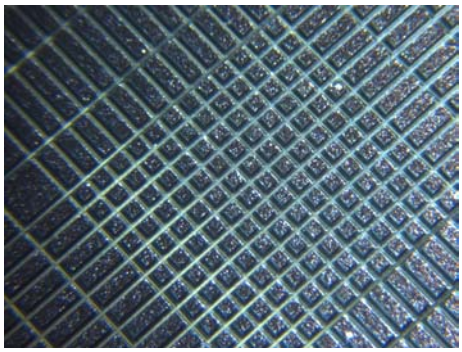


Fig. 1. Optical image of the backside diced wafers with the new 'Disco' saw

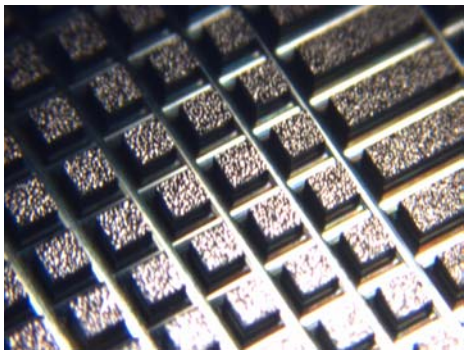


Fig. 2. Close up of the picture in Fig. 1

Polishing: Selected wafers were outsourced previously to a commercial service provider for polishing. Processing time was about two weeks at significant cost per wafer. We have therefore developed an improved in-house polishing procedure yielding maximum step heights between Si and glass sections of < 35 nm and a surface roughness in the range of a <5 nm (mirror finish). The step height variation is much better than those from the wafers polished by the commercial provider. The overall surface roughness, despite being far better than on all previous conventional wired UEA wafers, still requires improvement. Current experiments indicate that we will be able to accomplish a near sub nm scale surface roughness. We use mechanical polishing on emery paper of grit sizes 240 to planarize the wafer and polishing for mirror-finish is done on series of grits- 320, 600, 1200 using 6 micron nap paper. The final polish uses 50 nm alumina in a DI-water slurry.

Etching: Two new etching stations are being built to increase array throughout for the etching process.

Back side metallization: The metallization process was transferred to a second sputtering system to increase processing flexibility and reliability. A TMV Super Series SS-40C-IV Multi Cathode Sputtering system was optimized to be used for the UEA backside metallization. Furthermore, we have evaluated a new metal layer sequence with reduced layer thicknesses for the backside metallization in order to reduce processing time. The previous process uses TiW(150 nm)/Au (500 nm) with an additional TiW(100 nm) wetting stop layer. Layer stress and adhesion were characterized and optimized. Fig. 3 shows the bond pad opening in the nitride layer and Fig. 4 shows a single bond pad after metallization.

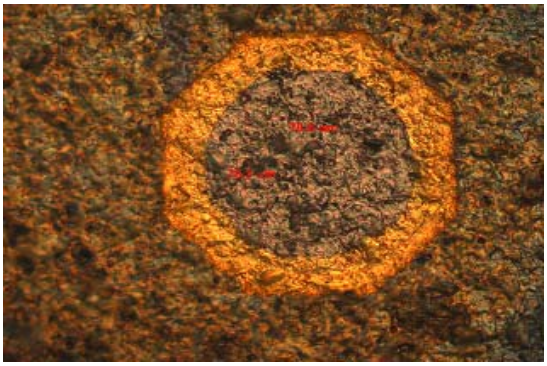


Fig. 3. Optical image of nitride bond pad opening

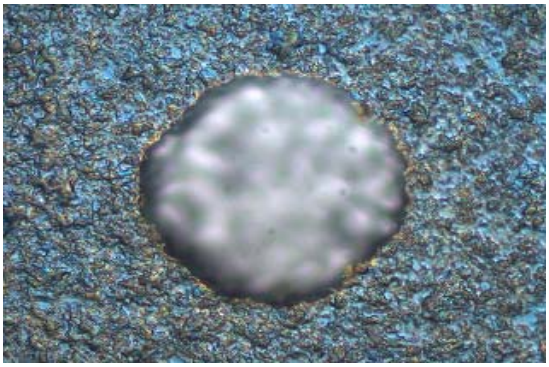


Fig. 4. Optical image of the bondpad after metallization

Previous processing challenges that impacted fabrication yield, such as the nitride and metal bond pad miss-alignment and metal-over etching were resolved. A new set of bright field masks were fabricated to improve alignment of different layers and make the process robust

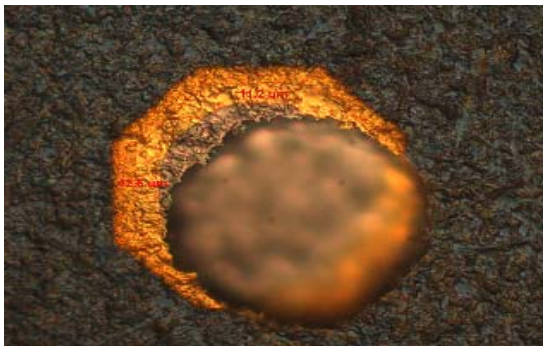


Fig. 5. Nitride and metal bond pad miss alignment

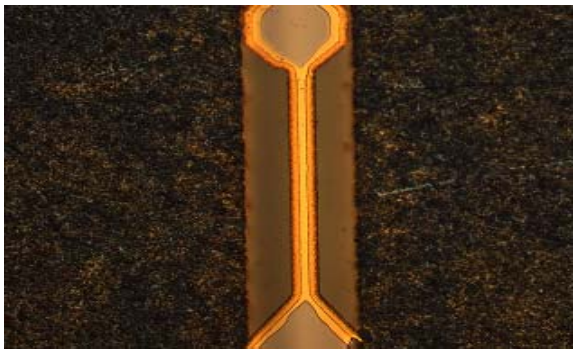


Fig. 6. Metal over etch for the SMD contacts and rerouting

A design of experiments (DOE)/failure mode effect analysis (FMEA) process was carried out to evaluate all prospective metal stacks for back-side metallization of the neural array and characterize different suitable metal layers in the new sputtering system. The main factors which affect the thickness and stress of a metal film are Argon pressure and sputtering power. The goal of the experiments conducted was to study the impact of power and process pressure on the stress and thickness of different metal films namely, Au, TiW, Ti, Pt. Tested output parameters were stress, layer thickness, resistivity and adhesion. A new, thinner metal layer stack Ti(50 nm)/ Pt(100)/ Au(200 nm) with an with an additional TiW(100 nm) wetting stop layer was characterized and optimized in the new sputtering system. The lift of process for different metal-stack thicknesses was optimized.

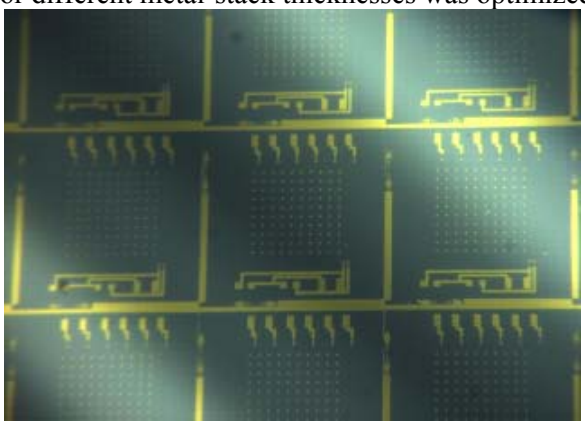


Fig. 7. Ti/Pt/Au Metal stack after lift-off

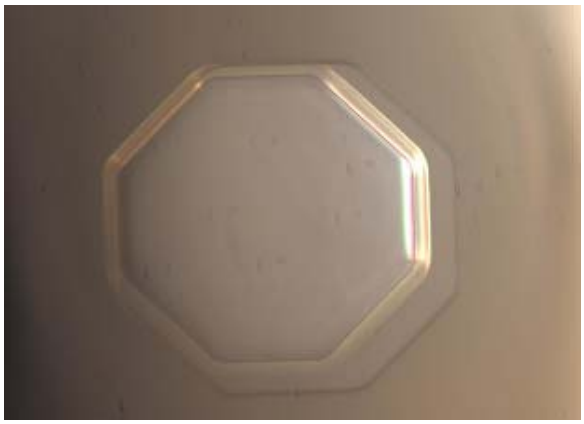


Fig. 8. Lift off pattern showing under-cut

Characterization of front side metallization: A DOE was performed to characterize the front side metal stack of Pt/Ti/Ir in the new sputtering system. These metals were characterized individually for thickness, stress, adhesion and resistively. Platinum thin films of 32 MPa compressive stress and Iridium of 39 MPa compressive stress were achieved. Titanium thin films with tensile stress were deposited yielding an overall metal stack of 18 MPa stress and a good adhesion. The total stack thickness is 412.5 nm. The metal stack passed scotch tape test which proves that adhesion is good. Furthermore, since in previous old generations of UEAs (prior to this contract) occasionally, unsatisfactory adhesion of the tip metallization on a few tips on selected UEAs was observed but never correlated to processing conditions, we have developed a new gel-pack based adhesion test and carried out initial experiments to check adhesion of metal on the tips of our current production UEAs. This test is supposed to yield additional, more realistic information on the metal adhesion on the sharpened electrode tips compared to conventional peel and ISO scratch tests. In this test, the metallized tips are pierced into a Fluoroware ® gel-pack tray repeatedly, thereby simulating the immersion into cortical tissue.

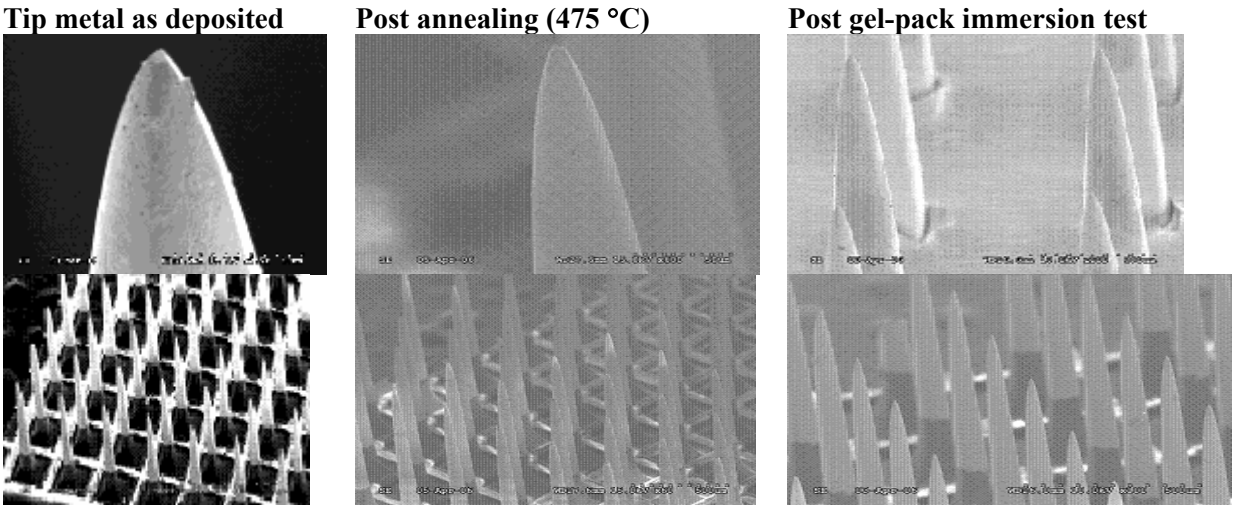


Fig. 9. SEM inspection of electrode tip metallization (top) and UEA overview (bottom) after deposition (left), after annealing at 475 °C and after gel-pack adhesion test (right).

Gel-Pack trays are normally used for shipping of microelectronics and MEMS chips. They make use of an adhesive gel that is fixed to the tray and adheres to the rough chip backsides during transport. The UEA tips were optically inspected before and after immersion into the adhesive gel using SEM. No obvious signs of delamination could be observed indicating sufficient adhesion of the metal on the tips. In future tests, we plan to implement a force gauge that will allow us to measure the pull force of the gel on the UEA during these tests.

Iridium activation: During the last quarter, we performed first successful activation processes for iridium metalized electrode tips. The UEA was wired to the new connector, consisting of two Hirose 50 pin connectors on printed circuit boards, held together by a metal mounting shell. Up to 24 electrodes can be activated in a single process using custom developed software and hardware. The impedances of all electrodes were measured using a BTI impedance tester. This device measures the voltage across the electrode when subjected to a 100 nA, 1 kHz sine wave. A 0 to 2 MΩ setting was used. Cyclic voltammetry (CV) was carried out with 1351 cycles at 1 Hz using a 1 V triangle wave and recording the device status every 100 cycles. The ADC of the current channel was set to a $\pm$5V range. After completing the activation process, the impedances on all electrodes were recorded using the same BTI device by directly probing pins on the adaptor board. Impedances ranged from 13 to 480 kΩ.

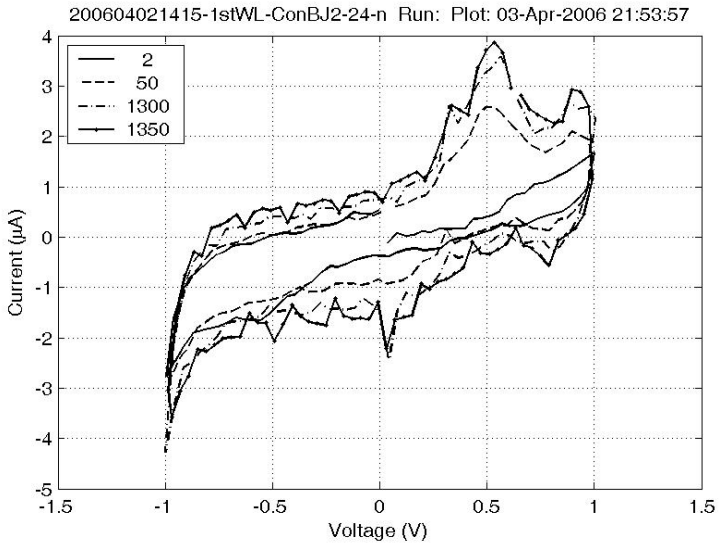


Fig. 10. Impedance of selected electrodes after iridium activation using cyclic voltammetry

Future Plans for Next Two (2) Quarters

About 30 additional arrays with backside metallization will be shipped to IZM for flip-chip bonding of the IC and the integration of SMD components. Wafer scale etching process will be developed. Soldering of wires for the wired arrays will be replaced with the wire bonding process.

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module consists of a single CMOS integrated circuit mounted on the back of the microelectrode array. We have received and tested both individual components and full functionality of the second version (INI2) signal processor chip in benchtop experiments. In addition to previous work we have started investigating the thermal characteristics of the device and the thermal impact on the nervous tissue as an attempt to later correlate it to histological data. As the first step towards evaluating the thermal impact of the integrated array on the brain tissue, the heat generation of the implanted array was simulated by means of finite element analysis using a simplified model.

Chip Redesign

The first chip, INI1 (Integrated Neural Interface, Fig. 11), has been thoroughly tested on the benchtop; a summary of its performance is presented in the previous reports. The new chip (designated INI2, Fig. 12) includes the following additions/improvements:

- On-chip bias current and bias voltage generators with digital calibration
- 10-bit A/D converter (was 9-bit on INI1 chip)
- Power coil voltage feedback using RF telemetry
- On-chip temperature sensor for monitoring tissue heating
- Robust command telemetry receiver circuits
- Programmable neural amplifier bandwidth
- Individual spike detection thresholds for each electrode
- 2× improvement in RF transmitter power efficiency
- Programmable RF transmitter power

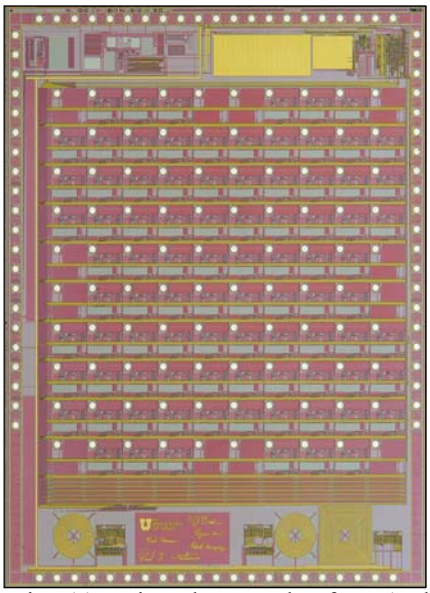


Fig. 11. Microphotograph of INI1 chip. The chip measures approximately 5 mm × 6 mm and contains over 30,000 transistors and 5,000 passive components.

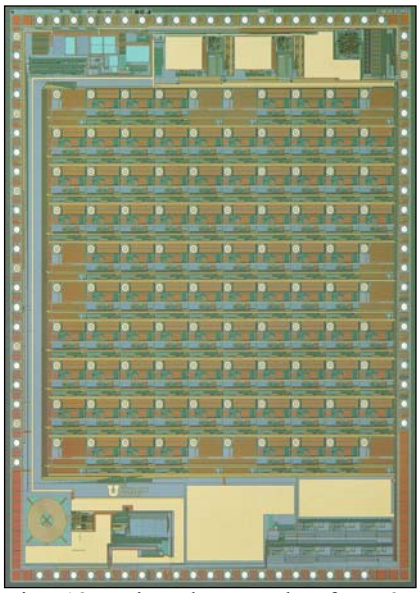


Fig. 12. Microphotograph of INI2 chip. The chip measures approximately 5 mm × 6 mm and contains over 63,000 transistors and 5,000 passive components.

The system level block diagram of chips is shown in Fig. 13. While the INI1 chip contained 30,000 transistors and 5,000 passive components (resistors, capacitors, and inductors), the INI2 chip features over 63,000 transistors and 5,000 passives. Testing of the INI2 chip commenced at the end of January 2006.

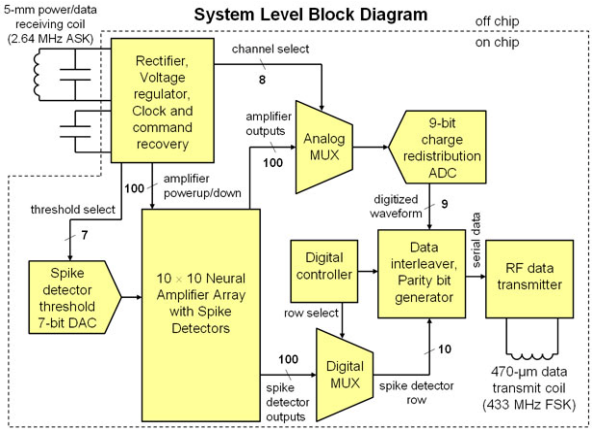


Fig. 13: System level block diagram of the INI1 chip. INI2 chip has a 10-bit ADC and individual spike-detection-threshold DACs for each electrode.

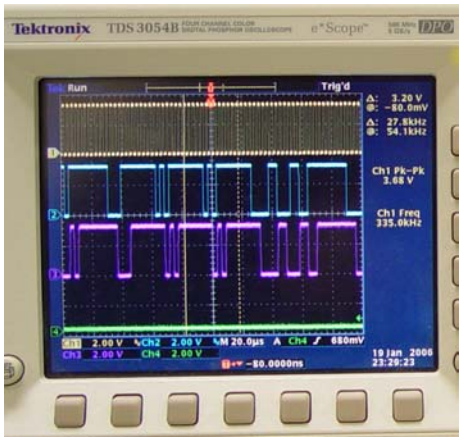


Fig. 14: Scope photo showing transmitted data from chip (blue trace, middle), received demodulated data (pink trace, bottom), and recovered clock (yellow trace, top).

Neural Data Telemetry Receiver

We have developed a system for receiving, demodulating, and interpreting the neural data streaming off the chip at 433 MHz using FSK (Frequency Shift Keying) modulation. We purchased an Agilent 4432B 3-GHz RF signal generator which is being used to simulate FSK transmission from the INI chip for controlled testing of the RF receiver. We also purchased an Analog Devices ADF7025 Demodulation Board that is capable of demodulating FSK signals in the 433-MHz range. We have successfully demodulated wireless telemetry signals from the INI1 chip in our lab using this board with a dipole antenna (Fig. 14). We built a microcontroller-based board to measure the BER (bit error rate) of the

received signal, and measure a BER of around 0.003 for a 13-cm separation between chip and antenna. However, the antenna matching network is currently optimized for 900 MHz instead of 433 MHz, so we expect some improvement in BER when we make this change.

The RF receiver is interfaced with another circuit board we have built to synchronize with and decode the telemetry packets from the INI chip, and transmit this data to a PC via a standard USB bus. We have successfully tested this board with another custom-written Graphical User Interface (GUI) using demodulated data streams (Fig. 15 and Fig. 16).

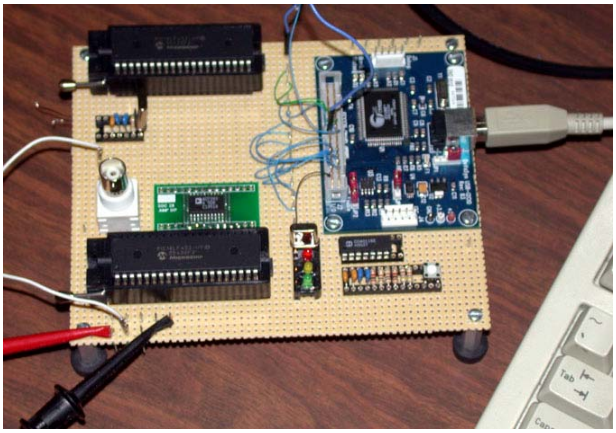


Fig. 15: PC USB interface board that will be used to connect the RF receiver front-end to a computer.

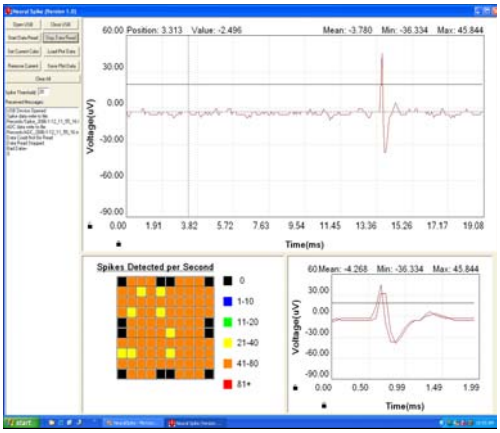


Fig. 16: Screenshot of custom-written GUI to receive and display neural data telemetry from the INI chip.

Simulation of power dissipated from the chip in brain: The power dissipation or the thermal impact of the implanted wireless neural interface electrode arrays on surrounding tissue was simulated under the assumption that the signal processor has a maximum power consumption of around 13 mW. This amount of power consumption/dissipation was observed during the bench top testing of the INIP1.

To investigate the thermal profile generated by the implanted integrated array, a finite element solver, Femlab (Comsol Inc.), was used. Steady-state power dissipation of the IC chip at maximum power consumption was assumed. The scalp was approximated as a thermal insulating barrier. The thermal properties of brain tissues used for the simulation were obtained from the literature [Duck 1990, Bowman 1975, Buse 1988, Valvano 1985, Connor 2004]. The simulation model takes into account conductive effects only and ignores further cooling effects caused by forced convection (e.g. blood circulation). Thus the temperature values given here should state an upper boundary for the maximum temperature/heating to be expected.

Below is the simulated result of thermal distribution in surrounding tissue of the array. Using the measured power consumption of the chip (13.5 mW over the chip volume of 6.552 mm^3), the simulation indicates that the temperature increase of the surrounding tissue in direct contact with the array can reach a maximum of 1.17 °C. In tissue more than 5 mm distant from the array, the temperature increase is less than 0.5 °C. This indicates that the anticipated power dissipation of the wireless array should not lead to any negative thermal effects on the nerve tissue. The simulation data is yet to be verified by experimental results. Such experiments are currently being designed. Existing literature data indicates maximum permissible temperature increases of ca. 1°C or maximum power densities of 80 mW/cm^2 of exposed tissue area [Seese 1998]. Other data [Ueda 1977] states that 0.64 W for a 3 mm diameter probe or temperatures greater than 47° C caused "spreading depression" in rats after 28 seconds of irradiation. In olfactory cortical guinea pig slices, aberrant activity began at 2° C over normal [Fujii 1982]. Our simulation data thus indicates that thermal effects may be small or negligible. We are currently preparing thermal imaging experiments with test devices to validate the simulation results.

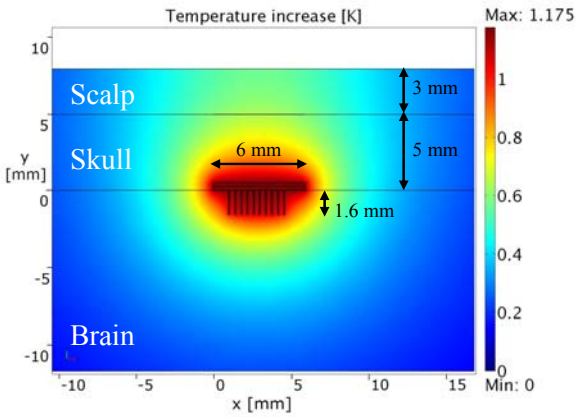


Fig. 17. Simulated temperature field created by wireless, integrated neural interface, implanted in brain tissue (13.5 mW of chip power).

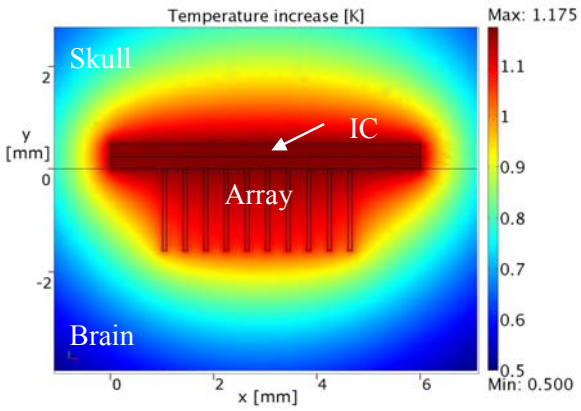


Fig. 18. Magnified view of simulated temperature field created by wireless, integrated neural interface, implanted in brain tissue (13.5 mW of chip power).

Future Plans

Testing of the INI2 chip is currently in progress. We have finished work on the external interface circuits introduced above, and adapting them to work with the INI2 system. We will use these external interfaces to interact with the packaged, coated INI devices to be used in animal experiments. The simulated results will be validated by experimental measurements using test structures. In addition, we will further refine the thermal simulations and complete test structures and an experimental setup to measure the actual temperature distribution of UEA test devices powered at between 1 and 30 mW in water and gel (as brain tissue substitute) using an infrared thermal imaging camera.

III.a.3 Task 3: Development and fabrication of PI and BCB coils

Description/Rationale

Additional coils on polyimide (PI) were manufactured and tested. The two layer coil with two 51-turn coils and 20 µm width as well as 15 µm spacing was selected for the assembly of the package. The work on the alternative solution based on BCB was halted, due to the good results which were achieved using the PI based coils.

Future Plans for Next Two (2) Quarters

Functional assembled modules will be built using the appropriate PI based coils.

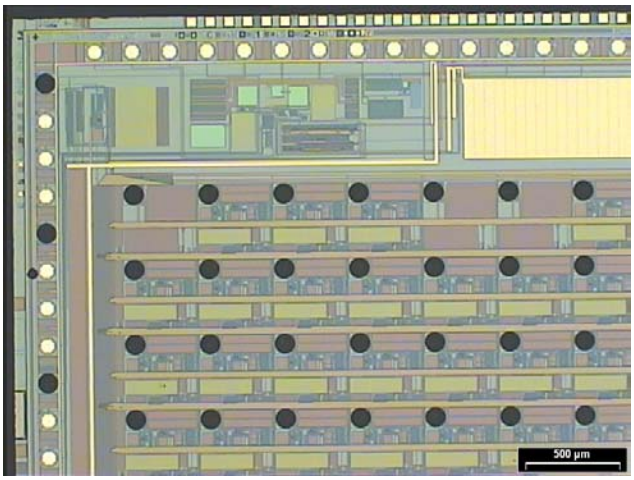
III.a.4 Task 4: Flip-chip bonding and assembly

Description/Rationale

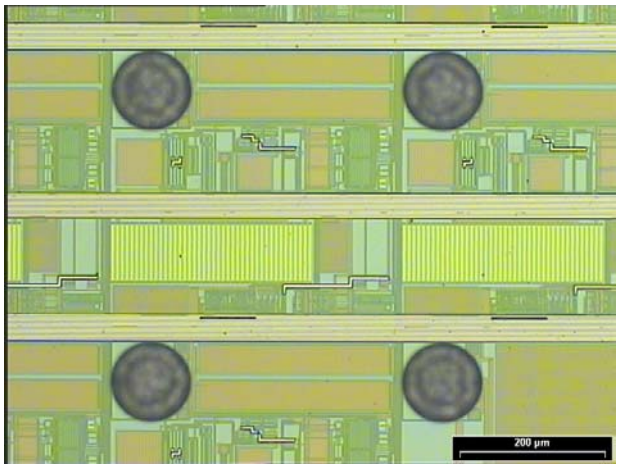
Single chip AuSn bumping is in progress with a redesigned bumping mask. The assembly process was successfully demonstrated using test chips and test arrays: test chips were Au/Sn bonded on test arrays, solder paste was dispensed and SMD as well as spacer components were reflow soldered, the ICs were underfilled, ferrite plates were adhesive bonded on PI based coils and the coil/ferrite components were finally adhesive bonded and soldered on the ICs back-side and the spacer.

Experimental Results

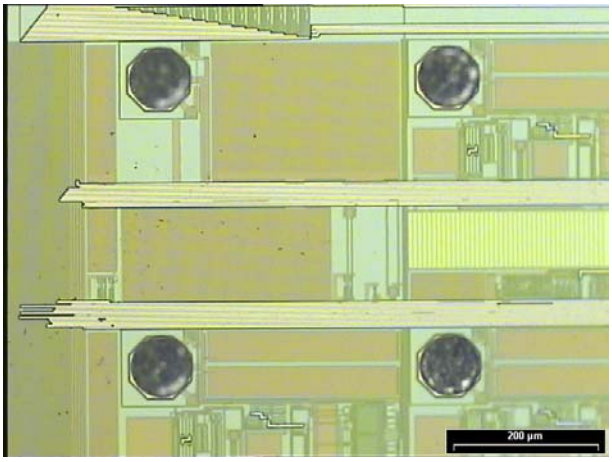
Au/Sn electroplating: Further 12 functional ICs have been Au/Sn bumped. They are now ready for dicing to separate the single chips from the substrates. Two chips per substrate were inserted. For the Au/Sn bumping the new redesigned mask was used. The overlap is now minimum 8 µm, with 97 µm bump diameter. Fig. 19 shows the bumps in detail. For comparison an old picture from bumps produced with the old mask is added.



a)



b)



c)

Fig. 19 Optical microscopy images after plating and etching using the new bumping mask (see (a) and (b)); (c) shows for comparison the Au/Sn bumps created by the previous mask

Assembly of the package: Ferrite plates were bonded on the PI based coils using adhesive. The coils were fixed on the chuck of a flip chip bonder, adhesive material (in our case the same material that was used for underfilling) was dispensed on the coils and the ferrite plates were adjusted to the coils. Following application of an appropriate bonding profile, the ferrite plates were glued to the coils. The new spacer components were successfully tested.

For the mounting of the coil/ferrite on the fully assembled and underfilled test module, underfiller was dispensed on the ICs back-side and solder paste was dispensed on the two spacer pads. Using a flip chip bonder the coil/ferrite was aligned to the package and bonded. A modified bonding process was developed to combine reflow soldering of the solder paste on the spacer and adhesive bonding of the ferrite on the ICs back-side at the same time. Fig.20 shows an optical microscopy image of a fully assembled dummy array and a cross section of the package. A remaining issue is the still comparably weak adhesion of the metallization layers on the array (see last quarterly report). The modified metallization stacks presented in this report should alleviate this problem and will be applied in the next batch of devices sent to Fraunhofer IZM.

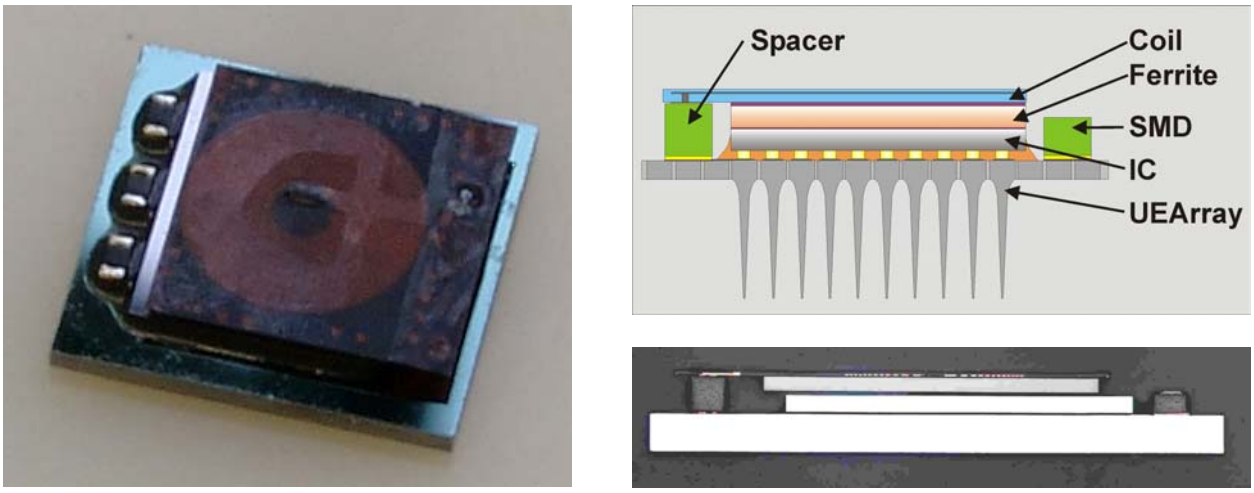


Fig.20. optical microscopy image of a fully assembled dummy package (left) and a cross section as well as a schematic of the functional package (right)

Discussion/Interpretation of Results

The assembly of the package was successfully demonstrated using test components for IC and array, despite the fact that the provided arrays had a weak adhesion of the pad metallization. Further Au/Sn electroplating process for the single chip bumping is in progress.

Future Plans for Next Two (2) Quarters

Arrays with changed polishing and grinding process as well as new pad metallization will be tested at IZM with respect to crack formation and adhesion of the metal layer. Redesigned ICs will be AuSn single chip bumped. An adaptation of the assembly processes will be necessary when changing to arrays with pins and a glass/silicon top surface. A further optimization of the bonding process of the coil/ferrite on the package will be performed. Finally, wireless UEAs using the INI2 chip will be assembled.

III.a.5 Task 5: Hermetic encapsulation and layer coating

Description/Rationale

Various surface treatments were tested to achieve good adhesion of parylene to the device materials. The surface treatment process was optimized.

Experimental Results

Parylene adhesion test: parylene films do not have strong adhesion to inorganic surfaces, such as metal or silicon. Si generally requires a primer or other surface treatments prior to parylene deposition to improve the adhesion of parylene to various surfaces. We compared the strength of the adhesion of the films to substrates from different surface treatments by using the ASTM standard D3359B - a standard method for measuring adhesion using a tape peel test. Scotch brand tape (#810, 3M Corp) was used to perform the adhesion test. According to ASTM D3359B, the adhesion test results were classified into six grades, where 5B represents the best adhesion and 0B represents the poorest adhesion.

Parylene was deposited on silicon substrates and stored in an environmental chamber for 2 hours prior to performing tape adhesion tests. Two environmental chamber conditions were used: 120°C, 100% relative humidity (RH) and 150°C, 100% RH. The good adhesion of parylene to the substrate following the 120°C/100% RH environmental test is an indicator that the encapsulation will be compatible with autoclave sterilization processes.

Discussion/Interpretation of results

The surface treatment vs. adhesion test results are listed in tab. 2. It was shown that an oxygen plasma followed by a dry silane A174 treatment produced the best adhesion on both silicon and silicon carbide

surfaces. The oxygen plasma serves two purposes: it cleans the substrate surface and provided hydroxyl groups on the substrate surface forming covalent bonds with the silane, thereby improve adhesion. The primer thickness also impacts the parylene adhesion.

Tab. 2: Adhesion test results.

Sample ID#	**0116A**	**0125A**	**0202B**	**0125B 0202A**	**0202C**	**0320**
Substrate	Si	Si	SiC	Si	Si	Si
Plasma	O_2 + Ar	Ar	O_2	O_2	O_2	O_2
Primer/ thickness	A174 /70nm	none	A174 /70nm	A174 /70nm	A174 /70nm	A174 /110nm
Test condition	120˚C / RH 100% 2 hrs	120˚C / RH 100% 2 hrs	120˚C / RH 100% 2 hrs	120˚C / RH 100% 2 hrs	150˚C / RH 100% 2 hrs	150˚C / RH 100% 2 hrs
Average classification	4B	4B	5B	5B	4B	2B

Future plans for the next (2) quarters

The combination of Parylene C and SiC as encapsulation layer showed good results in the leakage current tests as anticipated in our proposal. In order to further characterize and improve the encapsulation behavior, additional tests will be carried out to generate larger, statistically more relevant data sets that will allow long term process monitoring and control and serve as prerequisite for a potential later production and/or FDA approval.

The investigation of the adhesion of Parylene C on SiC with an adhesion promoter will focus on a dry application of the promoter. Dry application is necessary if the substrates do not allow immersion into wet medium (e.g. hydroscopic polymers and sensitive circuit parts). The results will be compared with the adhesion properties of the wet silane application.

Also, the adhesion between SiC and silicones as well as Parylene C and silicones will be investigated. For this purpose, medical grade silicones will be used to enhance the mechanical stability of the encapsulated integrated device. Surface modifications of the encapsulation films will be necessary to ensure a satisfied adhesive strength to silicone. For this, surface energy measurements will be performed.

III.b.1 Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

III.b.1.1 Bench testing of interface/electronics

We have completed benchtop testing of the INI1 chip. Our tests show basic functionality in all modules. Our voltage regulator successfully converts an ac voltage on a small off-chip coil into a regulated 3.3 VDC on-chip supply. The regulator requires a minimum peak coil voltage of 5.6 V for proper power supply generation. We are currently powering the chip via a 2.64-MHz wireless link in our laboratory. Command data may be sent to the chip by amplitude-modulating the power waveform. We have sent data at a rate of 6.5 kbit/sec, although we have discovered a bug in our data receiver that leads to prohibitively high bit error rates. The source of this bug is now well understood, and this circuit was corrected in the INI2 chip.

III.b.1.2 In-vivo testing of interface

Description/Rationale

The probe system has been tested in-vivo in rats.

Experimental Results

In January 2006, we tested the INI1 neural amplifier circuits with a Utah Electrode Array implanted in the barrel cortex of an anesthetized rat. Although the long (~30 cm) wires necessary to connect the array to the INI1 circuit board picked up significant amounts of 60 Hz noise (and other interference), we validated amplifier operation with real neural signals (Fig. 21).

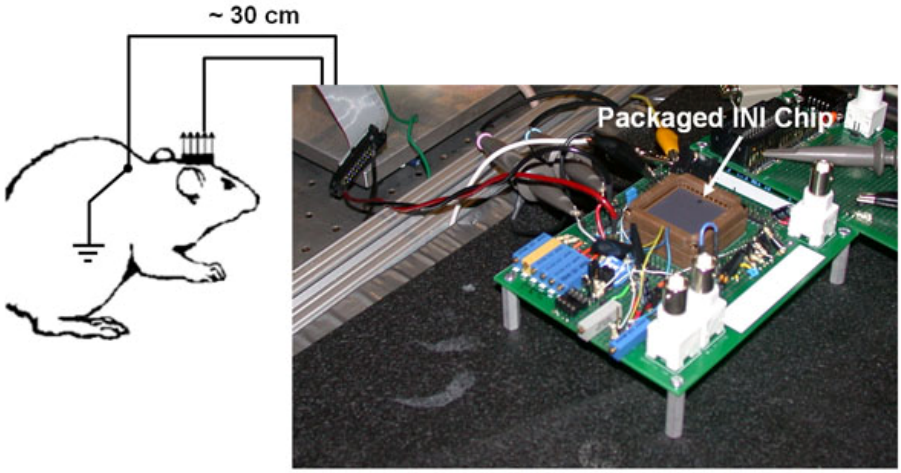


Fig. 21: Diagram of rat experiments. A 4 × 4 Utah Electrode Array was implanted in rat barrel cortex and attached to a packaged INI chip via ~30 cm wires.

To test the neural recording system, including amplifiers, spike detectors, and ADC, we used an arbitrary waveform generator to play back recorded neural data from Krishna Shenoy's lab at Stanford. The INI1 chip was powered wirelessly for this test.

Discussion/Interpretation of results

The neural signal amplifiers exhibit a proper gain of 60.1 dB, and a bandwidth ranging from 1 kHz to 5 kHz to isolate spikes. The input-referred noise of the amplifiers is 5.1 μV_{rms}. We consider this noise level acceptable, but we aim to improve this parameter in the next design. The cross-talk signals from non-selected recording sites is measured to be -64 dB. This clearly exceeds the performance requirements since it is 24 dB more than the -40 dB specification stated in the system requirements. Through external control, the multiplexer can be switched between electrodes in less than 1000 ms. Spike detectors function as designed, with a programmable detection threshold. The on-chip ADC works to 9-bit accuracy at a sample rate of 15 kS/s. The linearity of this circuit is excellent, with INL and DNL errors of less than ±0.8 LSB. The 433-MHz FSK data transmitter is functional, and we have demonstrated a received signal strength of -85 dBm using a half-wave resonant dipole antenna at a distance of 15 cm while using only the on-chip 54-nH inductor as the transmitting antenna. Power consumption measurements indicate that the entire chip consumes 13.5 mW of power.

Future plans for the next (2) quarters

Phase I (base contract period): We have ordered three chronic cats and are planning to implant them around the first of April, 2006. The INIP2 chips will be ready for connecting to the implanted animals by mid April, so we will have about two weeks to record responses using the (benchmark) Cerebus before we attempt to use the wireless system. This will also allow us to validate the performance of the surgery and the recording experiment prior to use of the wireless system and a later comparison of the wireless

system to the wired benchmark system. By the end of May, we expect to be able to document the performance of the INIP2 chip in one month of chronic recording in feline cortex.
Phase II (option I): We will be ready to conduct Phase II animal experiments once we have designed, fabricated and tested the INIP3 chip (third version INI chip). We expect that the engineering and design work will be done starting in summer 2006, and will be completed by November 2006. The chips will be sent to Fraunhofer IZM for integration with the UEA, and returned to Utah for encapsulation. We expect that by the start of 2007 we will be ready to implant Phase II cats.

IV. Concerns

During the 6th quarter of the project we observed a delay in the array fabrication due to an unanticipated performance shift (process parameters outside specifications) followed by a breakdown of selected thin film fabrication equipment, which rendered the backside metallization of the UEA wafers selected for the chronic recording experiments unsuitable for soldering or flip chip integration and resulting in a terminal loss of these UEA wafers. The subsequent processing of additional backup wafers (kept at an earlier production stage) caused a delay in the completion of UEAs for chronic recording and the implantation of the device in cats. As of April 3 we have implanted arrays in a cat for chronic testing. We are confident to be providing one month of recording data and continue with the project as scheduled, unless unexpected complications resulting from surgery or tissue response arise.
We have also transferred the thin metallization process to a new dedicated sputtering machine with strictly restricted use (see III.a.1, pp.4-5 of this report) in order to create redundancy of critical fabrication processes and to consequently mitigate processing risks in the future.

Salt Lake City, Utah, April 7th 2006

Prof. Dr.-Ing. F. Solzbacher,
Department of Electrical Engineering, University of Utah

V. References

[Duck 1990] Duck, F.A., *Physical properties of tissues*, Academic Press, 1990.

[Bowman 1975] Bowman, H.F. et al, Theory, measurement and application of thermal properties of biomaterials, *Ann. Rev. Biophysics-Bioengineering* 4, 48-80, 1975.

[Buse 1988] Werner, J., Buse, M., Temperature profiles with respect to inhomogeneity and geometry of the human body, *J. Appl. Physiol.*, 17-25, 1988.

[Valvano 1985] Valvano, J.W., Cochran, J.R., Diller, K.R., Thermal conductivity and diffusivity of biomaterials measured with self-heated thermistors, *Int. J. Thermophys.* 6, 301-311, 1985.

[Connor 2004] Connor, C.W., Hynynen, K., Patterns of Thermal Deposition in the Skull During Transcranial Focused Ultrasound Surgery, *IEEE Trans. Biomed. Eng.* 51 (10), 1693-1706, 2004.

[Seese 1998] T.M. Seese, H. Harasaki, G. M. Saidel, Cr. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue in chronic heating", Lab. Invest., vol. 78, no. 12, pp. 1553-1562, 1998.

[Ueda 1977] Ueda, M., Bures, J., Fischer, J. "Spreading depression elicited by thermal effects of ultrasonic irradiation of cerebral cortex in rats.", J. Neurobiol., 8, pp. 381-393, 1977.

[Fujii 1982] Fujii, T and Ibata, Y., "Effects of heating on electrical activities of guinea pig olfactory cortical slices". Pflugers Arch. 1982, 392, 257-260.